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(71) Applicant : **XEROX CORPORATION**
Xerox Square
Rochester New York 14644 (US)

(72) Inventor : **Lee, David D.**
3715 Redwood Circle
Palo Alto, California 94306 (US)
Inventor : **Bruce, Richard**
1956 Alford Avenue
Los Altos, California 94024 (US)
Inventor : **Lewis, Alan G.**
1610 South Mary Avenue
Sunnyvale, California 94087 (US)

(74) Representative : **Johnson, Reginald George et al**
Rank Xerox Patent Department, Albion House,
55-59 New Oxford Street
London WC1A 1BS (GB)

(54) AM TFT LCD universal controller.

(57) A universal, stand-alone controller integrated circuit (IC) for high resolution, active matrix liquid crystal displays (AMLCD's) incorporating the following features : (1) serial to parallel conversion of the refresh data stream to support vertically split panels as well as multiple scan drives, (2) data re-ordering to support various color pixel/filter arrangements including delta-triad RGB and quad RGGB color filter mosaics, (3) two-dimensional anti-aliasing image processing, (4) color/gray-scale correction/compensation due to change in operating temperature, and (5) host interface with programmable control registers to hold various display configurations and control parameters. With these features, the stand-alone AMLCD controller simplifies the graphics/display adapter design by providing a simple single-panel single-drive interface, similar to that of the CRT's but in digital formal, to various types of the AMLCD's. It also reduces the functional and performance requirements of the AMLCD panel driver IC's by integrating pixel data rearrangement otherwise implemented in the driver IC's, hence allowing more line drivers to be integrated within a smaller driver chip. The controller of the invention establishes a universal, standard interface between the host system and AMLCD's of various panel technologies, resolutions, and different timing requirements.

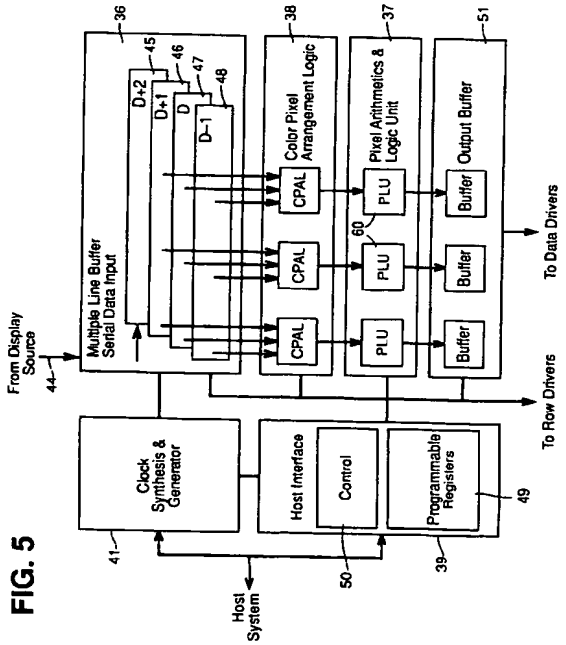

FIG. 5

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This invention relates to controllers for enabling or energizing flat panel, active matrix, liquid crystal displays.

Flat panel, active matrix (AM), liquid crystal displays (LCD) using thin film transistors (TFT) in series with each pixel element have become popular as TV displays or computer monitors. Color versions are also common, achieved by splitting each pixel into sub-pixel elements, each with its own color filter. Annexed Fig. 1 shows the main elements of a color display system with an active matrix liquid crystal display (AMLCD) panel as a single module 10. The panel 10 comprises a known matrix array 11 of liquid crystal display elements 12 with correspondingly positioned red, green and blue color filters (not shown). The array will contain many more elements than that shown, as will be clearer below. A display element, a pixel 13, consists of a thin-film transistor 14 (TFT) having a gate 15 and a capacitor 12 representing the LCD element. One electrode 16 of the TFT is designated its data line electrode 16. The intensity of colored light transmitted by each element is determined by a drive voltage applied to the pixel's data electrode 16 when the scan electrode 21 is pulsed high. See, for example, publications [1, 5] as well as US-A-4,716,403 for a description of a typical AMLCDs. Throughout this specification, numbers in square brackets refer to publications whose citations will be found in the annexed Appendix.

Two peripheral circuits driving the panel directly are a row driver 20 selecting a horizontal line 21 and a column driver 22 driving vertical data lines 23. As one horizontal line (row) 21 is selected, all TFT's 14 connected to the line are turned on and data driven by column drivers 22 is loaded into the pixel electrodes in parallel via conductors 23.

Most AMLCD modules 10 also include a separate LCD controller IC 25 which provides an interface to the row and column driver IC's 20, 22 from the display source driver, the host system's display adapter/controller 26, a separate module. The display adapter 26 usually consists of a RAM display data source (frame buffer) 27, and a programmable controller IC 28 to drive various displays with different configuration parameters. It may also includes a RAMDAC IC 29 (color look-up table with digital to analog conversion) to map a given color space into individual color components (RGB) which are then used to drive displays taking these as inputs. Most CRT monitors take the analog input as a standard data format, but most color TFT AMICD's take the digital RGB format.

The problem addressed is driving a high resolution AMLCD panel, which involves the lack of standardization in the pixel layout of the panel, the interface signals and timing requirements for the panel, the panel resolution, the number of displayable colors, and refresh frequencies or refresh scheme. This will be clearer from the following discussion. As can be seen in Fig. 1, the column driver IC 22 receives a video data stream from the display adapter 26 via the LCD controller IC 25. Many column driver IC's for AMLCD panels, especially for color TV's with panel size less than 3-6 inches diagonally, take analog inputs. As the display resolution increases, the pixel scan rate increases proportionally. This, in turn increases the input data sampling rate of the column driver as shown in Table 1 below:

TABLE 1 COLOR LCD with 60 Hz refresh rate (analog RGB)

DIPLAY	RESOLUTION	LINE TIME	PIXEL TIME (RGB PIXELS)
VGA LCD	3X640 x 480 (912,600 pixels)	34.72 µs	54.3 ns (17 ns)
Super VGA/XGA LCD	3x1024 X 760 (2,334,720 pixels)	21.93 µs	21.4 ns (7 ns)
Super-XGA LCD	3x1280 X 1024 (3,932,160 pixels)	16.28 µs	12.7 ns (4 ns)

As will be noted, with higher resolution panels, the output loads at the data terminal also increases, and hence the output driver circuit must be made larger to have a higher driving capability. Therefore, it becomes almost impractical to use analog inputs for high resolution (beyond the XGA) panels; see the description in publication [1]. Furthermore, it becomes very difficult to integrate high-voltage (above 8-10V) column drivers with high frequency sampling circuits at the input terminals on the same chip (i.e. hard to scale down with the shrinking technology). The fastest column driver IC's with a digital input currently available offer an input sampling frequency of about 20 MHz, whereas a 1024 by 768 panel would require an input rate of 50 MHz. Even with integrated TFT drivers on the panel, the input sampling rate will remain under 20 MHz [3].

A similar mismatch exists in high-resolution, passive Super-Twisted Nematic (STN) LCD panels and a common technique to resolve the mismatch is to split the panel into top and bottom halves. Data lines are separated in the mid-panel and driven from both sides with different column drivers. It effectively doubles the input band-

width without requiring high speed driver IC's at the cost of preparing a dual-scan data stream, but has a serious drawback as the panel resolution increases. Splitting the data (column) line in the middle of the panel makes data lines accessible only from one side. This leads to reducing testability and possible repairing of the panel prior to the encapsulation of the liquid crystal material, especially for defects caused by breaks in split lines. If both ends of the lines are accessible, the same defect may be tolerated by shorting the broken line outside the panel or providing drivers on both ends. To meet the input sampling requirements and to be more defect-tolerant, it would be more appropriate to split the panel vertically into left and right halves, rather than splitting it in top and bottom halves. Splitting the panel vertically does not require changing the panel layout. Only the drivers are loaded from the display adapter/controller, as if the panel were split in multiple planes.

Typically, the data stream into the display device is serial as prepared for the most common CRT display's pixel-by-pixel, single-scan drive interface. Low-cost DRAM's or multiported VRAMS's are the common storage for the refresh data, and high speed access (staticcolumn or page-mode in DRAM and serial-port in VRAM) to these devices usually provides a single, long serial data stream. It is not trivial to convert that long serial data stream to a parallel format suitable for vertically spilt panels. For example, the video (serial) port of the VRAM shifts out data serially from 512 or more serial shift registers loaded in parallel, so the data in the middle of the stream cannot be accessed until all previous data are shifted out. If the horizontal resolution of the vertically split panel is shorter than the depth of the shift registers, a special technique or a separate buffer is required to convert this serial data stream into the format needed by the vertically split panel. A software driver manipulating the frame buffer may re-arrange the data accordingly, but then it would become an undesirable, device-dependent driver.

The current AMLCD technology offers the potential for excellent image quality, which may ultimately exceed that obtainable with high-resolution CRT's. The source of the better imaging potential results from several attributes. A few among many are: (1) flexibility in defining the color-filter mosaics, including the size, shape, and luminance-profile of individual elements; (2) addressability (meaning how the elements are selected to create a line) and control of individual elements; (3) decoupling of the image-forming function from image-generating function, and others [4]. While it provides significant opportunities for a high quality displays, it present significant problems in producing low-cost, high performance AMLCD's. Several display parameters must be carefully chosen considering the panel technologies, the driver IC's, the source drivers, manufacturing cost and applications. This has been investigated by others using computer simulation methods or actually building the AMLCD's with various parameters [4, 5, 6, 7]. Among many different display parameters, the resolution, the number of gray levels on each addressable pixel and color filter mosaics, have been predominant factors in determining the image quality.

The panel resolution and the number of gray levels of each pixel element strongly depends on the panel technology and driver IC's. The choice of color mosaic usually depends on applications and also makes a great impact on image quality. Again, many researchers have done extensive studies to find an ideal color mosaic for a given panel resolution and the number of gray levels [4, 5, 6, 7]. Figs. 2(a)-(f) show various types of RGB color mosaics, where R, G, and B represent red, green and blue filter elements, respectively. The larger blocks represent pixels made up of the R, G, and B subpixels. While the majority of existing AMLCD's uses stripe RGB mosaics (both horizontal and vertical) arranged in many different ways, researchers have found that the delta-triad and quad-green mosaics would produce superior image quality [4]. Some column driver IC's provide a special function to re-arrange the data format inputted according to the color mosaic of the panel, but the types of mosaics are limited (usually stripe RGB or variants) due to complexity of data re-arrangement required for some special mosaics, such as delta-triad or quad green. The data pattern of these two color mosaics is harder to generate than others since a color pixel spans over two scan lines. A buffer holding a line of display image must hold the data over two scan line times and scramble the RGB to generate the data stream correctly for these two mosaics. A column driver would require three input buffers per two output drivers for the quad-green mosaic, and one more level of buffering would be necessary to hold the data over two scan lines. It would be inappropriate for the display adapter to do this pixel rearrangement since the color mosaic is also panel or application specific. No currently-available controllers provide a solution to this problem.

Another big problem confronting color AMLCD image quality is the presence of spatial quantization or aliasing artifacts that manifest themselves as jagged edges or stair-steps [8]. A number of software and hardware algorithms resolving this problem have been implemented in different levels of the display system, mostly for CRT's, and some of them are being considered for application to the AMLCD's [9]. The algorithms may vary among different AMLCD configurations such as different types of color mosaics. The implementation of the algorithm may be done in the display controller/adapter or even at a higher level in the software drivers. But this is not a cost-effective solution.

Some environmental factors, such as temperature and light, can noticeably affect the image quality of the TFT AMLCD. For example, an increase in temperature increases both the on and off current of the pixel TFT.

While the increase in on-current is beneficial to faster display operation, the increase in off-current reduces the pixel data storage time. Combined with the liquid crystal's temperature-dependent characteristics, it may result that operating temperature changes the gray-level of the LCD, as depicted in the transmission versus applied voltage curve for different temperatures shown in Fig. 3 [10]. A correction requires a temperature sensor and digitizer, temperature detection logic, and special logic to properly adjust the gray-level. Since the temperature effect is closely tied to the TFT technology and LC material (thus panel technology specific), the correction must be done in the display module set for the correct thermal characteristics of the panel, provided by the manufacturer. This is a costly solution which remains panel technology specific.

These are some examples of the different kinds of requirements imposed on the controller whose function is to receive the video signal and re-order the data for driving a particular AMTFTLCD.

Prior art solutions include integrating the controller within the display/graphics sub-system, such as a VGA board, with the result that the controller is only usable with that particular display system. Some stand-alone controllers are also available, but they are rather simple, providing only synchronizing clocks and buffering of a few pixel data, and support only the simpler mosaics. Color image enhancement features and the various color pixel arrangements are usually carried out by special graphics adapter boards and separate matrix driver ICs with limitations. This approach is costly and requires extra hardware, and is not a good solution. See, for example, US-A-s4,926,166; 4,275,421; and the Hitachi HD66300T horizontal driver chip for TFT-type LCDs. The support they provide is very limited, for example, CRT or LCD, or different sized displays, or several simple color filter mosaics.

Thus, there is a need in the art for a flexible, versatile stand-alone interface controller to allow interfacing to the widest possible range of AMTFTLCDs from various systems.

An object of the invention is a universal AMLCD controller implementing features to solve the problems discussed in the previous section.

Another object is a hardware architecture of an AMLCD controller integrating the aforementioned features to interface to the widest range of high resolution AMLCD's from various host systems.

A further object is a programmable AMLCD controller that will take a single-panel single-drive data stream and re-arrange the data stream as programmed for different types of panels, hence providing a very simple interface to the display adapter.

Still another object is a separate controller with a flexible buffer for re-arranging the data to match the RGB color mosaic of an AMLCD, whereby its column driver and its interface can be greatly simplified.

Another object is an AMLCD-specific controller with buffers to hold adjacent pixels' data and to provide data rearrangements for both vertically split panels and different types of color mosaics.

An object of the invention is an AMLCD controller with a special logic circuit to implement local, two dimensional image enhancing algorithms cost-effectively.

Still a further object is an AMLCD programmable controller which provides temperature correction at a reasonable cost and possessing a flexible way of controlling the correction.

In accordance with one aspect of the invention, there is provided a controller according to claim 1 of the appended claims.

In accordance with another aspect of the invention, there provided a controller according to claim 3 of the appended claims.

In accordance with a further aspect of the invention, there is provided a controller according to claim 5 of the appended claims.

In accordance with a further aspect of the invention there is provided a controller according to claim 7 of the appended claims.

In accordance with still another aspect of the invention, there is provided a controller according to claim 11 of the appended claims.

Preferably, the means under user control for re-ordering the video data comprises a multiple line buffer. Preferably, the multiple line buffer is capable of storing four scan lines of video data. Preferably, the re-ordering will allow simultaneous driving of vertically split parts of the LCD.

The single chip controller may further comprise means for two-dimensional image quality enhancement of the video image represented by the inputted video data.

The single chip controller may further comprise means for modifying the gray scale of pixels at image transitions in accordance with the intensity of surrounding pixels.

The single chip controller may further comprise means responsive to the operating temperature of the LCD for compensating for changes in LCD properties. In this embodiment the under user control for re-ordering the video data comprises internal programmable registers.

Preferably, the line buffers are each divided into plural modules.

The means under user control for re-ordering video data may further comprise a first buffer, a multiplexer,

and a second FIFO buffer serially arranged.

Preferably, the image quality enhancement means comprises multiple lookup tables for weighted averaging of pixel intensity, and an adder of the weighted values.

The single chip controller may further comprise a temperature detector and an additional lookup table for modifying pixel intensity to compensate for temperature changes.

With these features, the stand-alone AMLCD controller simplifies the graphics/display adapter design by providing a simple single-panel single-drive interface, similar to that of the CRT's but in digital format, to various types of the AMLCD's. It also reduces the functional and performance requirements of the AMLCD panel driver IC's by integrating pixel data rearrangement otherwise implemented in the driver IC's, hence allowing more line drivers to be integrated within a smaller driver chip. Therefore, the controller of the invention as a single chip establishes a universal, standard interface between the host system and the AMLCD's of various panel technologies, resolutions, and different timing requirements, and thus renders the display/graphics sub-system design independent of the display panel technology, and vice-versa. The controller chip can reside in either location, namely, the display adapter board in the host system, or on the display module in the display.

The present invention will be better understood from the detailed description given herein below in conjunction with the accompanying drawings, which give by way of illustration only and not by limitation, a preferred embodiment in accordance with the present invention, and in which:

Fig. 1 is a block diagram of a system incorporating a controller in accordance with the invention;

Figs. 2(a)-2(f) show various color filter arrangements employed in AMLCDs;

Fig. 3 is a graph showing the transmission characteristics versus applied rms voltage of a super fluorinated LCD element at different temperatures;

Fig. 4 is a block diagram of the AMLCD Module;

Fig. 5 is a detailed block diagram of just the controller of Fig. 4 alone;

Fig. 6 is a detailed block diagram of the multiple line buffer of the controller of Fig. 4;

Figs. 7(a)-7(b) are, respectively, a view of the two-dimensional array used for anti-aliasing, and a detailed block diagram of the color pixel arrangement logic used in the controller of Fig. 4; and

Fig. 8 is a detailed block diagram of a pixel arrangement and logic unit used in the controller of Fig. 4.

The present invention provides a universal architecture for a stand-alone controller that provides a standard interface for active matrix, thin film transistor, liquid crystal displays (AMTFTLCD). The novel architecture offers the advantages, among others, that it simplifies the design of display/graphics adapters and reduces the functions required of AMLCD driver ICs, permitting more such drivers to be integrated within a single chip.

Features of the controller include the following: (1) a high speed digital interface to the host, with multiple line buffering and internal register-programmable configurations; (2) color and gray-scale image enhancing, such as subpixel averaging over time and space (anti-aliasing); (3) support for a variety of color pixel arrangements; (4) generation of control signals and data re-ordering for the matrix driver ICs.

A system block diagram of the controller 25 of the invention is illustrated in Fig. 2. A conventional display panel of the color TFT AMLCD type is schematically shown at 10. This can be one of many well-known color pixel arrangements as shown in Fig. 2, such as quad RGGB, triad, and stripe RGB pixels, and has been described in detail in the published patent and scientific literature and further details are unnecessary to comprehend the present invention. The panel 10 is typically provided with row drivers 20 for scanning and with column drivers 22 providing the video information or data. The input to the column driver 22 is digital RGB signals, and thus the column drivers 22 will incorporate conventional buffers and D/A converters.

The present invention has to do with the controller 25 which receives certain digital video, control, and sync signals from, for example, a host computer or TV receiver (not shown) and functions to organize the data and supply the data with the usual control and sync or clock signals to the panel drivers 20, 22.

In brief, the single chip controller 25 of the invention provides a local line buffer 36 which is capable of being written to and storing several (m) lines of pixel data to be annotated and displayed. A pixel arithmetic and logic block 37 computes the spatial pixel averages, reorders the data to be sent to the driver IC's. A color pixel configuration block 38 rearranges the pixel data according to the color filter implemented by the specific color matrix LCD 10. An internal host interface block 39 includes programmable registers to store various display parameters and configurations. A conventional phase-locked loop (PLL) 40 and clock (CLK) generator block 41 provide synchronization and control signals for the driver IC's. The video MUX block 42 multiplexes the second video signals to the line buffer to display alternate display sources in real time. Except for the conventional circuitry, such as the PLL 40 and CLK generator 41, the remaining blocks are described in greater detail below. The video MUX circuit 42 and the PLL 40 are not essential to incorporate in the single controller chip of the invention, and if desired their functions can be provided by separate chips.

As shown in Fig. 5, the multiple line buffer (MLB) 36 receives high-speed, serial input data stream from a display source 44, line by line, and stores them in the four (m=4) buffers 45-48 for a few line times, to be used

by the pixel arithmetic and logics unit (PLU) 37. The color pixel arrangement logic (CPAL) 38 together with conventional decoders (not shown) of the MLB controls the data being fetched from the MLB to match the color mosaic chosen of the AMLCD 10. The PLU 37 fetches a set of pixel data in the format necessary for vertically split panels when used, and performs anti-aliasing image processing to enhance the image quality and/or temperature correction. The host interface logic 39 includes a set of programmable control registers 49, 50 and the interface to the host system or off-chip ROM to program or load registers with various configuration and control parameters. The clock generator 41 generates synchronizing clocks and control signals for both row and column drivers 20, 22 as well as internal clocks. The output port 51 buffers the data to be sent to the driver IC's and controls the data transfers to match the data transfer format required by the driver IC's.

The MLB 36 includes four line buffers 45-48, each holding the data needed by column drivers to drive one horizontal line. Each line buffer (Fig. 6) consists of banks of small, independently addressed RAM modules 52, each holding a segment of the line data. The access unit of each RAM module is the data width of the RGB color components. For example, a suitable number of RAM modules 52 for each line buffer, that can accommodate the various RGB mosaics of Fig. 2 and the resolutions of Table 1, is 4. A typical line data segment is 3 X 320 pixels, and a typical access unit is 4 X 3 X 8 bits (8 bits per color component).

It will be understood that, in order to rearrange a serial input data stream into a parallel format, a buffer holding at least two horizontal lines must be present. One buffer receives the input data stream while the other provides the output data stream. With a line buffer comprising a number of smaller RAM blocks 52, arranged as shown in Fig. 6, when receiving the serial input data, only one module 52 per line buffer 45-48 is accessed at a time. When sending out the data to the N-column drivers 22, N modules are accessed simultaneously. The line buffers switch their roles as the scan line changes. The MLB 36 implements this by using pointers 53 to keep track of the order of the line, instead of moving buffered data among the line buffers. Two extra line buffers are provided--a total of four--to hold the data of two adjacent scan lines, to allow two dimensional anti-aliasing processing using an array (3X3) of pixels, in a manner known as such in the art.

To support various pixel mosaics including the delta triad (Fig. 2(e)) and quad-green (Fig. 2(f)) color mosaics, the size of the line buffer must be modular since the buffer may hold the data for two scan lines as in the cases of those two special mosaics. The operation of the MLB 36 is programmable by the means shown at 49, 50 to handle the difference in the input and the output scan frequencies in the case of the quad-green mosaic. The MLB's interface 39 to the display adapter (inputs to the MLB) remains the same regardless of color mosaics. The MLB 36 receives the display data one pixel (in RGB components) at a time serially, and sends out the data at the speed matching the data rate required for the flick-free refresh.

The CPAL unit 38 controls the access and re-ordering of the data being read out of the MLB, as programmed according to the panel mosaic being driven. As a result, the controller 25 of the invention hides the panel-specific control and data rearrangements, and thus provides a simple and universal interface to the host system. The data format sent to the display panel is thus controlled by the CPAL unit 38 in conjunction with the programmable registers 49. The CPAL 38 controls the decoders of the MLB such that the color pixel components in the right sequence are read out, rearranges them if necessary, and sends them to the PLU 37 in the correct order. It also fetches and buffers appropriate adjacent pixel components to be used by the PLU for anti-aliasing.

In a preferred embodiment shown in Fig. 7, the CPAL 38 comprises a controller 55 and a number of identical datapaths (N when the panel is split N ways vertically). The controller reads the programmable registers 49 and generates the addresses and control signals for the MLB and the datapath. The datapath includes an input buffer 56, three FIFO buffers 57, and multiplexors 58 in between the buffers, to rearrange the data format. The input buffer 56 latches one or two adjacent (horizontal) color pixel data (three RGB components) as illustrated in Fig. 2(b) and composes the data sequence in the panel's color component order. The FIFO buffer 57 holds 3 by 3 color component data fetched from three adjacent line buffers in the MLB 36 in horizontal order. Each element in a FIFO buffer represents one color component of the RGB components of eight adjacent color pixels. All nine components (see Fig. 7(a)) are fed simultaneously to the PLU, but the center element, designated P(i, j), is the current component being displayed in the panel. Adjacent components are used for anti-aliasing processing. The CPAL 38 sends out one set of data (nine components) at a time, and together with the PLU 37 it implements the highly pipelined operation to meet the refresh rate requirement.

Similarly to the CPAL unit 38, the controller 25 of the invention includes N units 60 of identical PLU's 37 to implement two dimensional -anti-aliasing of the display images, and-to perform temperature correction of gray scale on individual color components. See Fig. 8. The number N here is the number of scan drives required by the panel when divided in N vertical ways. Each PLU 60 consists of several lookup tables (RAM's) 61-64 and an adder tree 65. The lookup tables are read/write RAM, so some parameters of the anti-aliasing algorithms as well as temperature correction are programmable for specific applications. The PLU 37 supports the anti-aliasing algorithms based on a 3 by 3 pixel kernel. See Fig. 7(a). Both the anti-aliasing (lookup tables 61-63)

and the temperature correction (lookup table 64) can be performed on each color component independently.

Much of anti-aliasing research has focused on methods of creating lines or edges that appear smooth on raster displays. These known anti-aliasing algorithms frequently employ gray-scale to create a luminance distribution or filter across a line or an edge. These efforts smooth the jagged appearance of diagonal lines by lessening the effect of the discrete steps produced on matrix display panels. A reasonable and efficient approach is to band limit the digital images by the quantized gray-scale or luminance levels. The anti-aliasing algorithm supported by the PLU 37 incorporated in the preferred embodiment of the invention maps a spatially oriented luminance profile to the underlying pixel array (3x3), by calibrating the gray level of each pixelrelative to adjacent pixels. Typical luminance profiles that can be employed are Gausian, linear, and trapezoidal line spread functions. It should be noted that the method of spatial band limiting with the Gaussian luminance profile is a discrete approximation of the way in which the Gaussian electron beam in a shadow-mask color CRT serves to band limit spatial frequencies before they are sampled by the RGB phosphor dots at the CRT faceplate. These kinds of algorithms are described in the referenced publications [9, 10].

Fig. 8 shows the hardware elements of each PLU unit 60. As nine color component data are fed in, they are separated in three different weight groups, diagonally adjacent components, perpendicularly adjacent components, and the center component. The nine components values are used to access three corresponding lookup tables 62, 61, 63 to fetch their weighted contributions, and the adder tree 65 computes the weighted average of the center component. The content of the lookup tables is programmable and algorithm specific for the given pixel kernel and computing structure. The pixel kernel structure is also programmable within the maximum limit of 3x3 pixels.

The computed pixel component value 67 and current operating temperature information obtained from a known temperature sensor 68 are then used to access another lookup table 64 holding data to be used in correcting the gray level. The current temperature information selects the corresponding segment of the table divided in different temperature segments, while the pixel value selects the temperature adjustment value within the segment. The temperature adjustment value may not be uniform along the transmission curve, and thus the component gray value is further divided into several different regions as shown in Fig. 3. The last adder 69 in the PLU adds or subtracts the temperature adjustment value to or from the original value. The operation of the PLU 60 is controlled by programmable registers and both anti-aliasing and temperature correction may be turned off partially or fully depending on application.

The host interface 39 (Fig. 5) includes a byte-wide, parallel port that can be connected directly to the data bus of a host processor. The host processor may be of any type of controller or microprocessor. The host interface 39 has an internal controller (not shown) handling data transfers in and out of the programmable registers, and may use an external PROM to program the registers. The host interface port consists of byte-wide data bus, address but, and data transfer control signals.

All programmable registers incorporated in the controller 25 are read/write accessible, and grouped into four different categories to hold parameters of: (1) display configuration (e.g. panel resolution) (2) pixel configuration (e.g. color mosaic), (3) anti-aliasing (e.g. pixel kernel), and (4) temperature correction (e.g. lookup table organization). These parameters are used in various blocks as described above to generate correct data format and control signals for the panel and driver IC's, respectively. The specific circuitry to implement this is straightforward and will. be evident to those skilled in this art from the foregoing specification teachings.

Summarizing, while the AMLCD technology offers a significant opportunities for a high resolution, high quality display, it introducing serious problems in producing low-cost, high performance AMLCD's. The combination of several technologies that makes the AMLCD technology exceed the CRT technology in obtaining higher quality displays, for example, the panel technology, row and column driver IC's, packaging and assembly of panel and drivers, and display adapter/controllers, is what brings about the problems. As the panel technology advances, the problems multiply as a larger and higher resolution display becomes available forcing other designs, such as driver IC and display adapter, to change. To make such changes cost-effective and to raise the quality of an overall display system, the AMLCD controller of this invention implements various features that could otherwise be implemented in other parts of the system but at a significantly higher cost. Data reordering and pixel mosaic rearrangements vary among different panel technologies and it will be almost impractical to implement them in either driver IC's or display adapters/controllers. But, a local memory on a single chip to buffer a few adjacent lines provides a simple interface to the host system, while flexible and fast accesses are available to the display for various data format changes. Buffering of a few lines also provides the opportunity for image processing using a small but two dimensional pixel array, at a reasonably low cost. The temperature correction is often done in the display adapter, which is undesirable since it makes the adapter/controller technology dependent. With a minimal hardware addition, the adjustment to the temperature change can be done easily and accurately. Most importantly, the controller of the invention establishes a programmable interface to various types of the AMLCD's, and can thus become a standard and universal way of

driving AMLCD panels correctly and efficiently.

The controller of the invention is not limited for its image enhancement or anti-aliasing feature to the algorithm described using the 3x3 array and an averaging scheme for determining the intensity of each pixel along a line or an edge. Due to the multiple line buffer memory provided, this image enhancement scheme can in general use known algorithms which substitute in certain scan lines pixel element values derived from values stored in previous or subsequent lines and follows naturally from the presence of the multiple scan line buffer store. This aspect of the invention is also not limited to specific algorithms. The enhancements will be mainly used in overcoming jaggy or staircase appearance of lines and edges on these raster displays. It ultimately boils down to fixing the gray-scale intensity level for each pixel, especially at color or area transitions. Examples of suitable algorithms are described in publications [8, 10]; and in publications by Hewlett-Packard describing their Laser Jet Resolution Enhancement Technology (RET) system.

Also, while the split screen driving feature has been described in connection with a two-way, left and right half split, it will be understood that it is straightforward by upward scaling to implement a controller that will support more split screens than two, e.g., six for XGA-resolution, and the invention is not limited to a two-way split screen.

It also will be understood that the invention is not limited to incorporation of all of the various features as described herein in a common, single chip, stand-alone controller. To the extent that the prior art allows, the invention contemplates a controller chip incorporating each of the features alone, as well as various combinations of the features, though it is recognized that the full gamut of advantages is not realized in the absence of one or more of the features. Nevertheless, incorporation of one or several features still represents, to the best of our present knowledge, a decided improvement over currently-available AMLCD controllers.

To implement the controller of the invention as a single chip is a straightforward task using conventional IC processing. The individual circuits themselves are well known in other contexts, and are readily provided combined in a single chip in the same manner as they would be as a separate chip.

For completeness' sake, the contents of the cited references in the Appendix, and that of the other patents/publications referenced herein are hereby incorporated by reference.

While the invention has been described and illustrated in connection with preferred embodiments, many variations and modifications as will be evident to those skilled in this art may be made therein without departing from the spirit of the invention, and the invention as set forth in the appended claims is thus not to be limited to the precise details of construction set forth above as such variations and modifications are intended to be included within the scope of the appended claims.

APPENDIX

REFERENCES

[1] Y. Miyata et al., "Dynamic Characteristics of LCD Addressed by a-Si TFTs", SID '88 Digest, pp. 314-317, 1990.

[2] Y. Kanaya, "Problems in driver LSI resolved by low-voltage, single-source power supply", Flat Panel Display '91 Digest, pp. 168-172, 1991.

[3] A.G. Lewis et al., "Polysilicon TFT Active Matrix LCD drivers", SID '91 Digest, pp. 535-538, 1990.

[4] L.D. Silverstein et al., "Effects of spatial sampling and luminance quantization on the image quality of color matrix displays", Journal of Optical Society of America, Vol. 7, No. 10, pp. 1955-1968, October 1990.

[5] M. Takakura et al., "An Image Quality Simulation System for Matrix-Addressed Display Panels", SID '89 Digest, pp. 135-138, 1989.

[6] K.G. Freeman, "Simulation of Liquid Crystal Colour TV Displays", Euro Display '90 Digest, pp. 116-119, 1990.

[7] H. Martino et al., "Horizontal Stripe Color Arrangement for Large-Size TFT-LCD", SID '90 Digest, pp. 400-403, 1990.

[8] F. Crow, "The Aliasing Problem in Computer-Generated Shaded Images", Communication of The Association for Computing Machinery, Vol. 20, No. 11, pp. 799-805, November 1977.

[9] A.R. Jacobsen, "Determination of the optimum gray-scale luminance ramp function for anti-aliasing", in Proceedings of the SPIE/SPSE Conference on Human Vision: Methods, and Applications, 1990.

[10] Fujimoto et al., "Jag-Free Images on Raster Displays", IEEE CG & A, December 1983, pgs. 26-34.

Claims

1. A controller for an active matrix TFT LCD comprising:
   (a) an input for receiving a video data stream formatted as a sequence of serial lines,
   (b) buffer memory means connected to the input for storing a plurality of adjacent lines of the data stream,
   (c) means connected to the buffer memory means far re-ordering the video data into a format for parallel outputting to drive a selected LCD having one of a plurality of color subpixel arrangements, said subpixel arrangements including a delta and quad arrangement of the plural calors.

2. The controller of claim 1, wherein the subpixel arrangements further include horizontal, vertical, diagonal and staggered stripe subpixel arrangements.

3. A controller for an active matrix TFT LCD comprising:
   (a) an input for receiving a video data stream formatted as a sequence of serial lines,
   (b) buffer memory means connected to the input for storing a plurality of adjacent lines of the video

data stream,
(c) means connected to the buffer memory means for re-ordering the video data into a format for parallel outputting to a selected LCD for simultaneously driving vertically split parts of the LCD.

4. The controller of claim 3, wherein the LCD is vertically split for driving purposes into left and right halves.

5. A controller for an active matrix TFT LCD comprising:
(a) an input for receiving a video data stream formatted as a sequence of serial lines,
(b) buffer memory means connected to the input for storing a plurality of adjacent lines of the video data stream,
(c) means connected to the buffer memory means for re-ordering the video data to provide two-dimensional image quality enhancement for parallel outputting to a selected LCD.

6. The controller of claim 5, wherein the reordering is into a 3x3 array of pixels, and further comprising weighting means for modifying the gray scale of the center pixel of the array as a function of the intensities of the surrounding pixels in the array.

7. A controller for an active matrix TFT LCD comprising:
(a) an input for receiving a video data stream formatted as a sequence of serial lines,
(b) buffer memory means connected to the input for storing a plurality of adjacent lines of the video data stream,
(c) means connected to the buffer memory means for re-ordering the video data to compensate for changing temperatures and for parallel outputting to a selected LCD,
(d) means connected to the means of element (c) for detecting changing temperatures.

8. The controller of any of the preceding claims, wherein the controller comprises a single integrated circuit chip.

9. The combination of the controller of any of the preceding claims and the selected LCD.

10. The combination into a single chip of the controllers of claims 1, 3, 5 and 7.

11. A single chip stand-alone controller for an active matrix TFT LCD comprising:
(a) means far receiving serial video data,
(b) means under user control for re-ordering the video data into one of a plurality of formats each corresponding to what is required for driving a different arrangement of color subpixels in a selected LCD, said different arrangements including horizontal, vertical, diagonal, delta triad, and quad green color subpixel arrangements.

FIG. 1

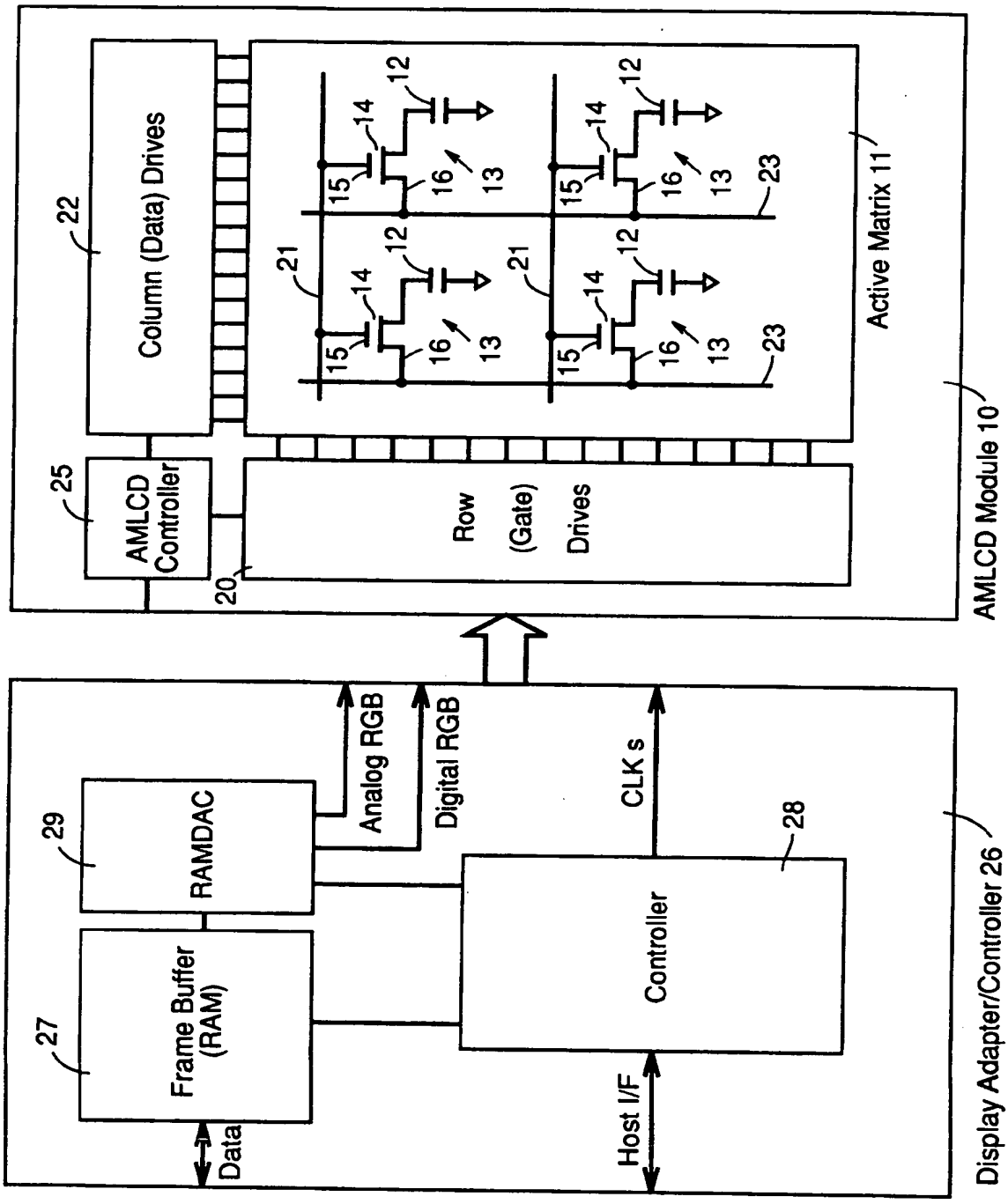


FIG. 2a

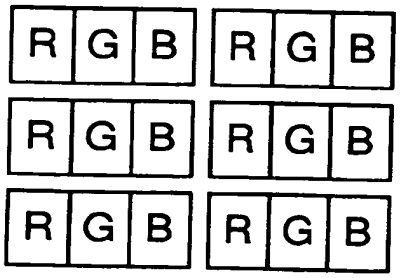


FIG. 2b

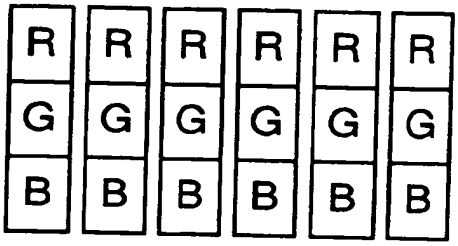


FIG. 2c

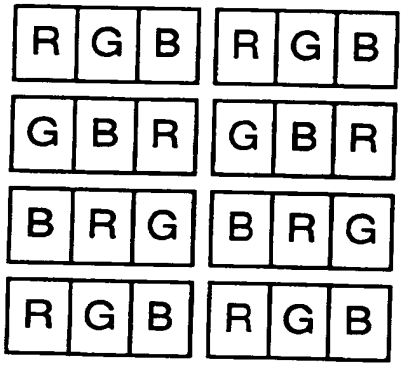


FIG. 2d

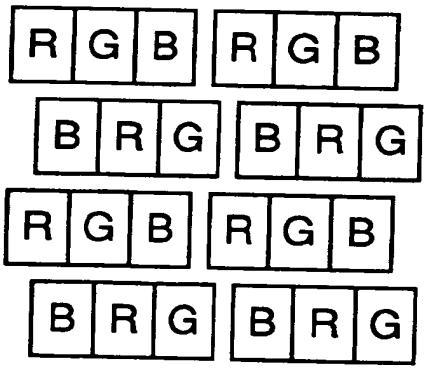


FIG. 2e

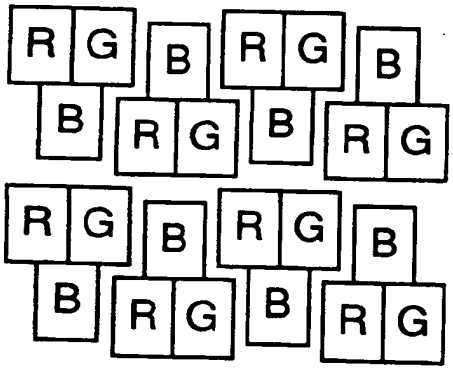


FIG. 2f

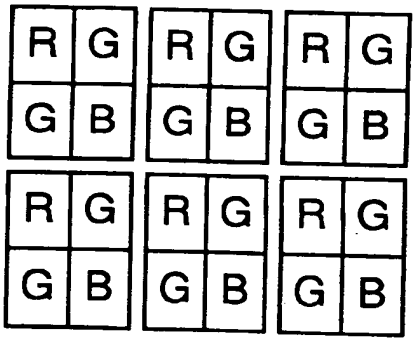
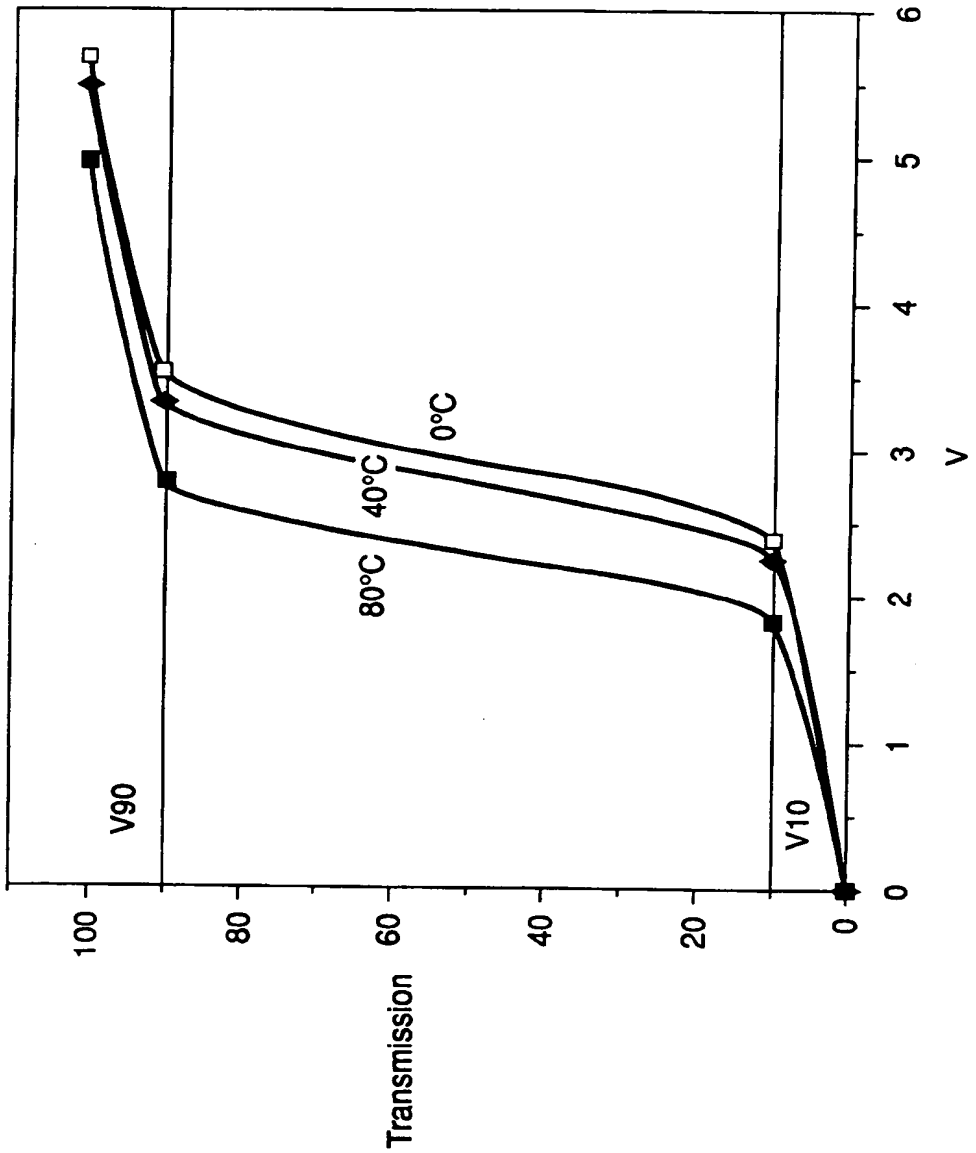


FIG. 3



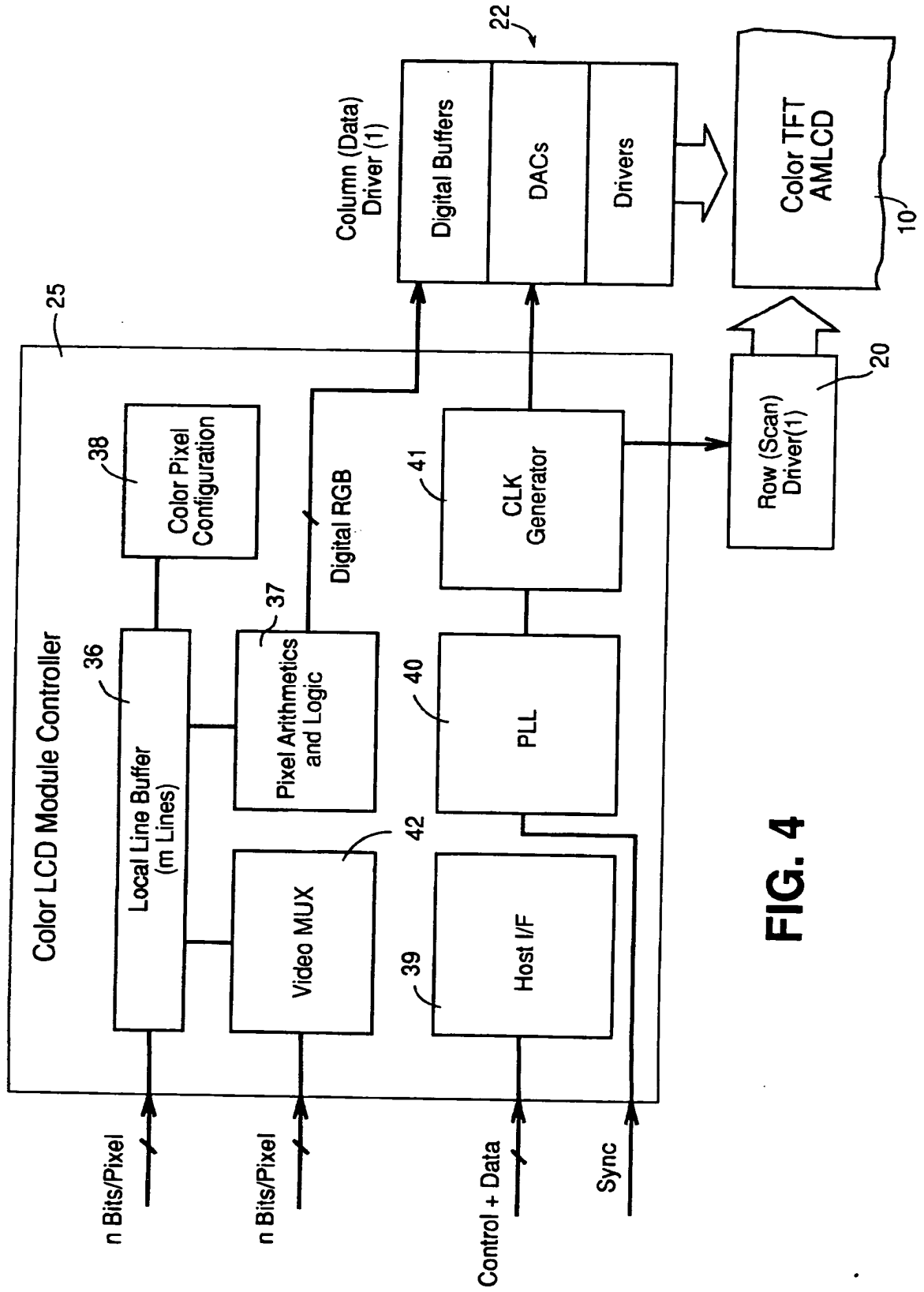


FIG. 4

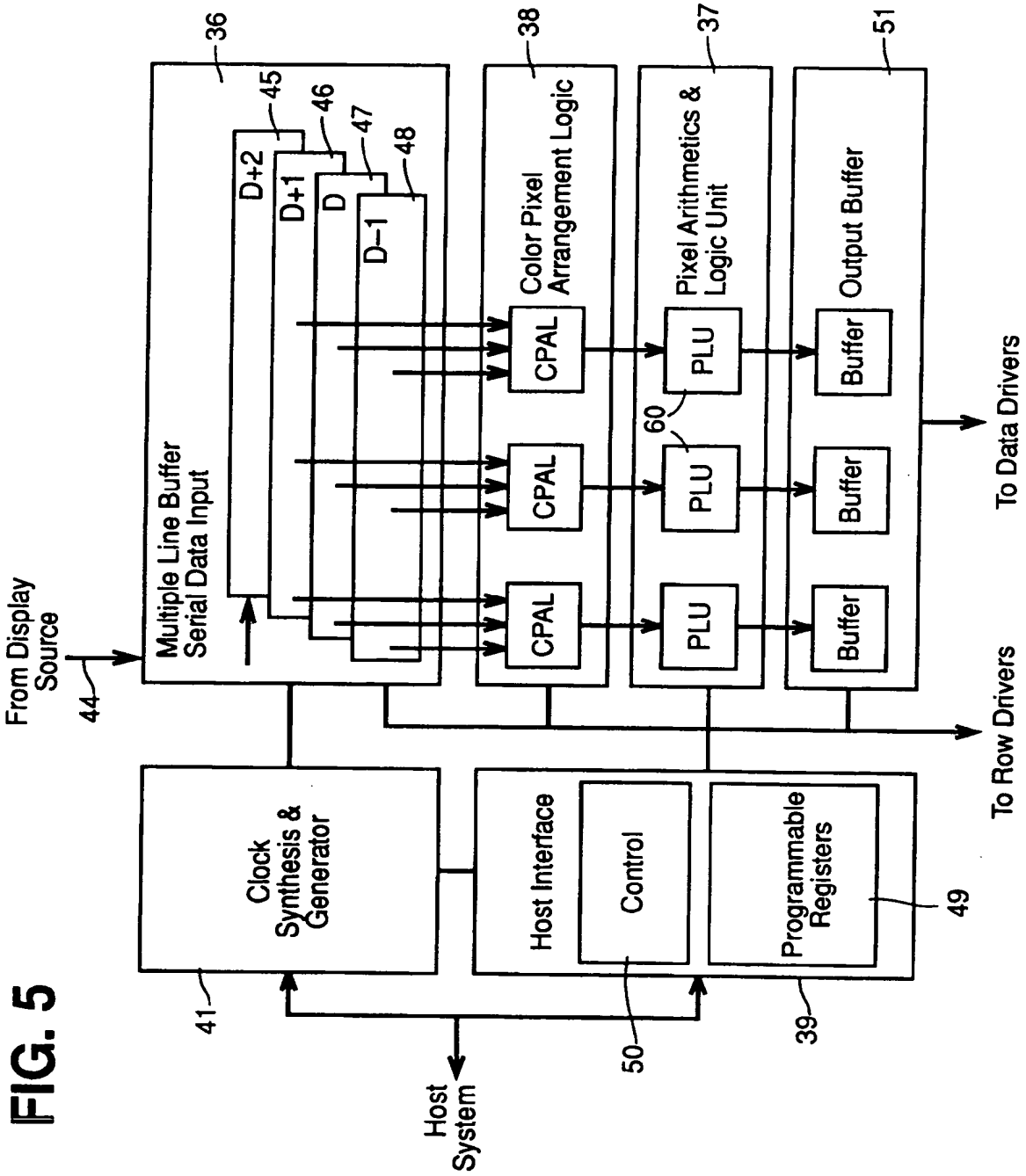


FIG. 5

FIG. 6

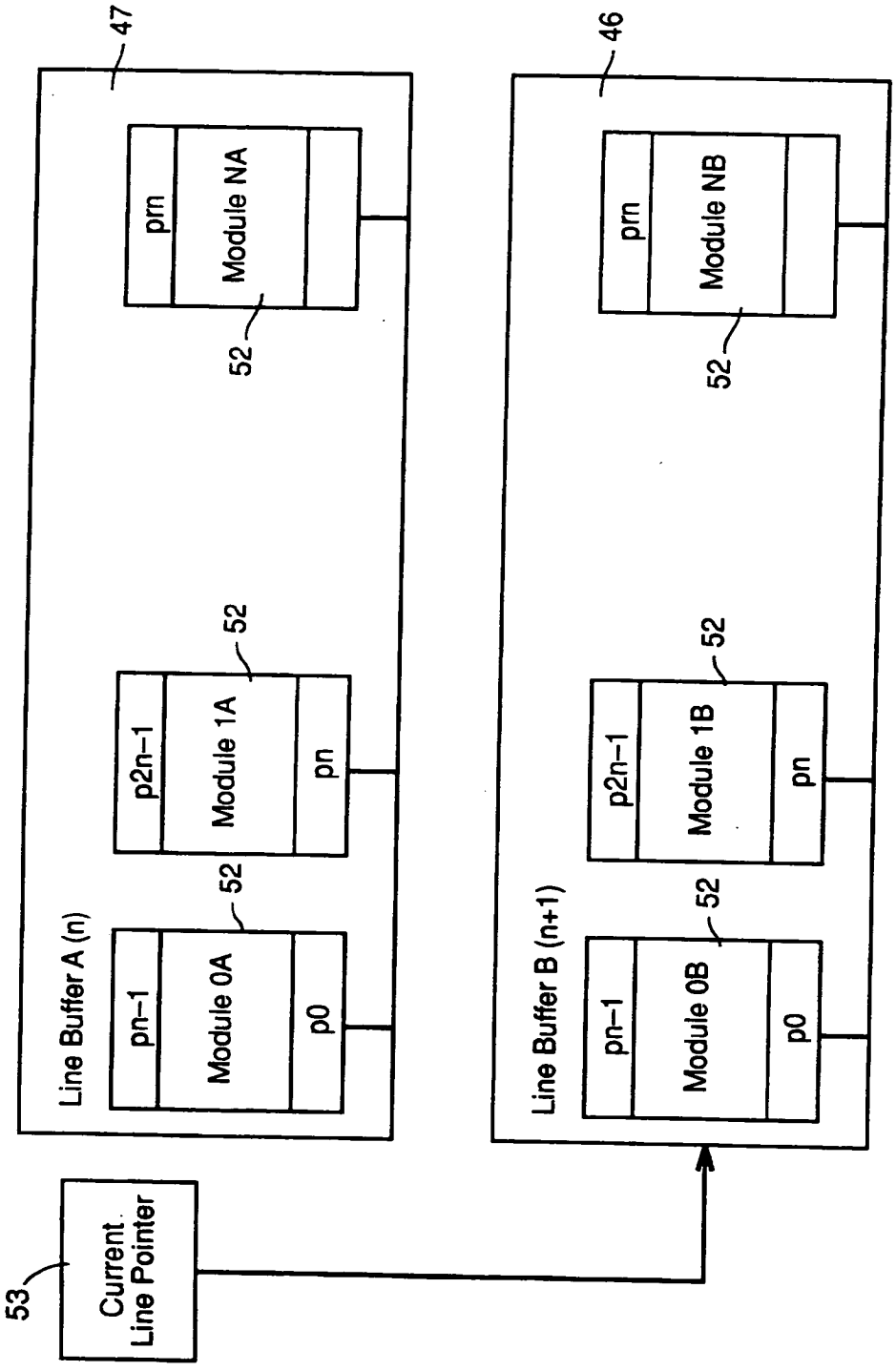


FIG. 7a

P(i-1,j-1)	P(i-1,j)	P(i-1,j+1)
P(i,j-1)	P(i,j)	P(i,j+1)
P(i+1,j-1)	P(i+1,j)	P(i+1,j+1)

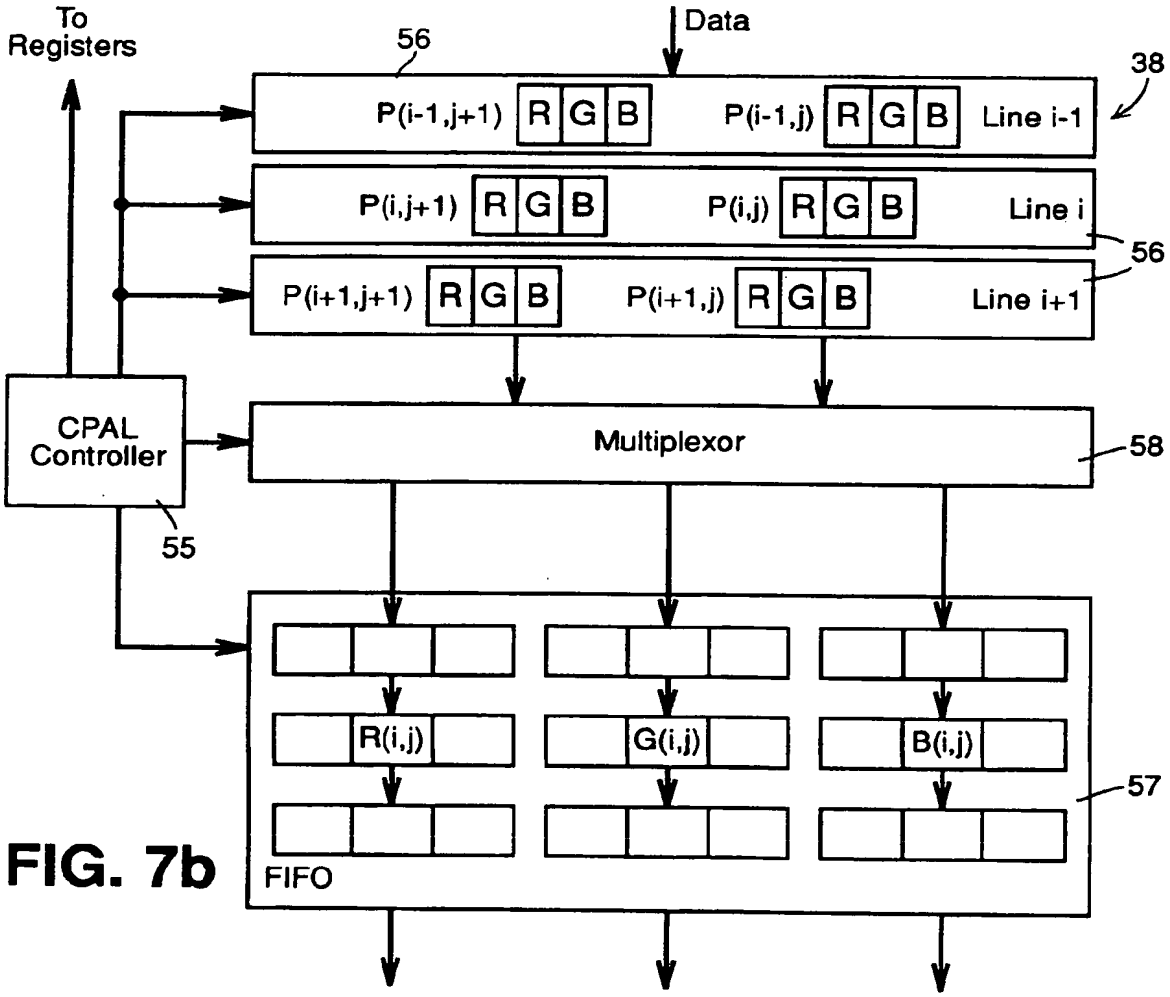


FIG. 7b

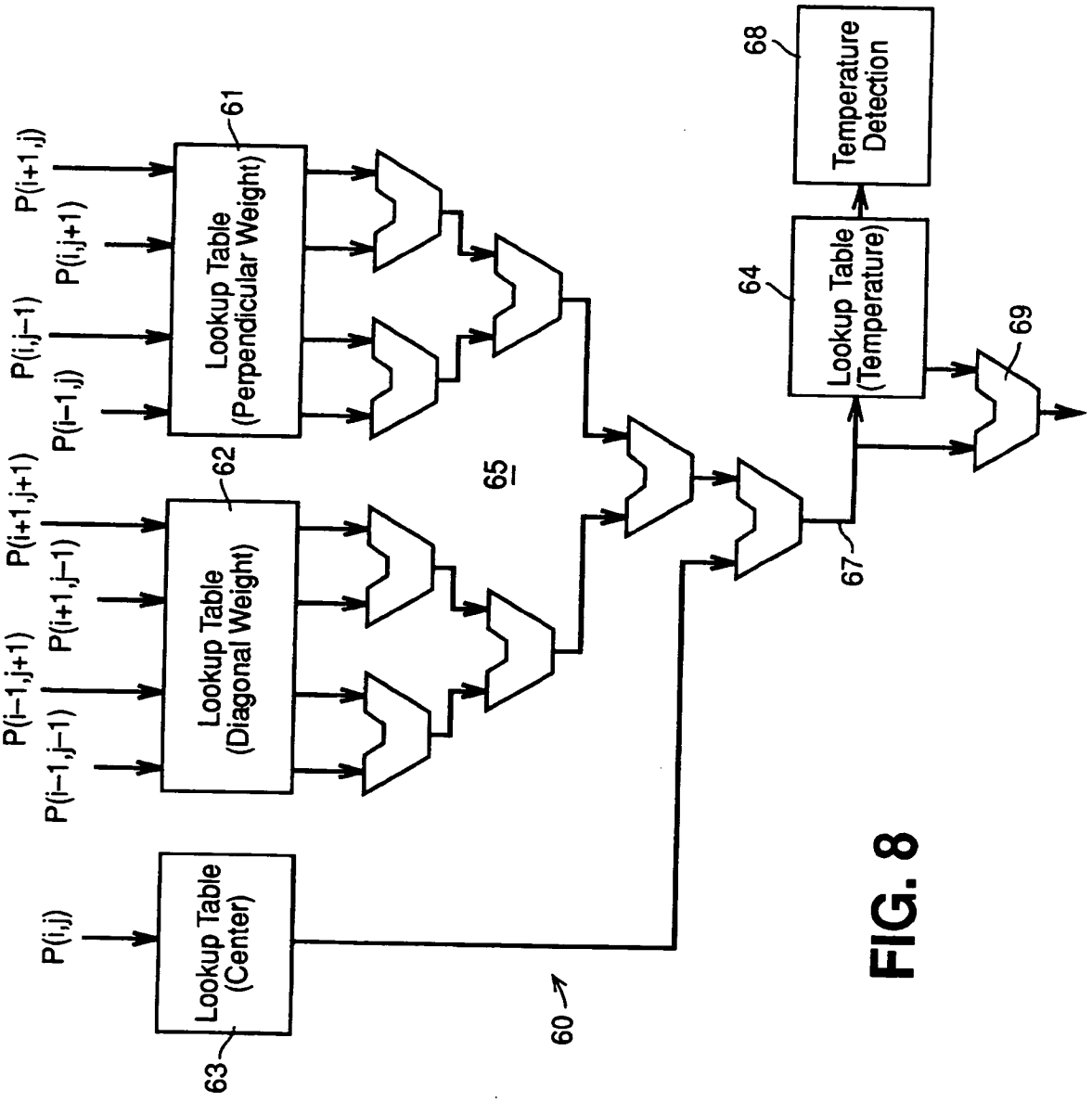


FIG. 8

European Patent Office

EUROPEAN SEARCH REPORT

Application Number EP 92311122.3

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	EP - A - 0 256 927 (COMM. A L'ENERGIE ATOMIQUE) * Abstract * --	1	G 09 G 3/36
X	EP - A - 0 213 630 (CANON) * Abstract; fig. 1 * --	1	
X	EP - A - 0 238 867 (CANON) * Abstract * ----	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 02 F 1/00
G 09 G 3/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	22-03-1993	KUNZE

CATEGORY OF CITED DOCUMENTS

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